Document made available under the Patent Cooperation Treaty (PCT)

International application number: PCT/US05/004429

International filing date: 14 February 2005 (14.02.2005)

Document type: Certified copy of priority document

Document details: Country/Office: US
Number: 60/544,719
Filing date: 13 February 2004 (13.02.2004)

Date of receipt at the International Bureau: 17 March 2005 (17.03.2005)

Remark: Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b)

World Intellectual Property Organization (WIPO) - Geneva, Switzerland
Organisation Mondiale de la Propriété Intellectuelle (OMPI) - Genève, Suisse

1293479

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

March 08, 2005

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE.

APPLICATION NUMBER: *60/544,719*
FILING DATE: *February 13, 2004*
RELATED PCT APPLICATION NUMBER: *PCT/US05/04429*

Certified by

Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

PTO/SB/16 (10-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EV 332955081 US **Date of Deposit: February 13, 2004**

INVENTOR(S)

Given Name (first and middle if any)	Family Name and Surname	Residence (City and either State or Foreign Country)
Vincent W.	Leung	San Diego, CA
Prasad S.	Gudem	San Diego, CA
Lawrence E.	Larson	La Jolla, CA

TITLE OF INVENTION (500 characters max)

ADAPTIVELY BIASED RF AMPLIFIER USING A POWER DETECTOR CONTROL CIRCUIT

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

☒ Customer Number **26263**

Type Customer Number here

OR

☐ Firm *or* Individual Name					
Address					
Address					
City		State		ZIP	
Country		Telephone		Fax	

ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* 7 ☐ CD(s), Number

☒ Drawing(s) *Number of Sheets* 12 ☒ Other (specify) Postcard, American Express Payment Form

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☒ Applicant claims small entity status. See CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees

☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number: **19-3140**

☒ Payment by credit card. Form PTO-2038 is attached:

FILING FEE AMOUNT ($)

$80.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract numbers are:

Respectfully submitted,

SIGNATURE K.W. Buckley

Date: February 13, 2004

TYPED or PRINTED NAME: Kevin W. Buckley

REGISTRATION NO. *(if appropriate)* 45,901

Docket Number: 60021010-0036

TELEPHONE 314.259.5817

USE ONLY FOR FILING A PROVISIONAL APPLICANT FOR PATENT

TITLE OF THE INVENTION

Adaptively Biased RF Amplifier Using a Power Detector Control Circuit

CROSS-REFERENCE TO RELATED APPLICATIONS

Not Applicable.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable.

REFERENCE TO A CD APPENDIX

Not Applicable.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to adaptively biased radio frequency amplifiers using a power detector control circuit and an adaptive bias method for radio frequency amplifiers based on the use of a power detector control circuit.

2. Description of the Related Art

In order to accommodate high data-rate transmission for the third generation (3G) wireless communication, spectrally-efficient variable-envelope modulation schemes are employed. The hybrid phase-shift keying (HPSK) adopted for the wideband CDMA (WCDMA) standard is one example. Spectral regrowth due to the transmitter circuit distortion is to be strictly limited. This often translates to stringent and challenging linearity requirements for the radio frequency (RF) amplifiers, which locate at the very end of the transmitter chain and are tasked to handle the highest signal levels.

Another important, although conflicting, design criteria is the amplifier power consumption. Since RF amplifiers consume a significant share of the battery power in a mobile device, their power efficiencies have a direct and determining impact on the talk time. Further complicating the issue, not only should the efficiency be maximized at the peak power level (without compromising the amplifier linearity), it should also be kept high during power backoff. It is because in, for instance, the WCDMA standard, power control (attenuation) is continuously and adaptively enforced so that the strengths of the transmit signals arriving at the base station are equalized regardless how far the mobile devices are.

In summary, the amplifier should exhibit high *average* efficiency to prolong battery life. The amplifier's bias should be adaptive: For small signal condition, the quiescent current

should be kept to its minimum to enhance the efficiency. For large signal condition, the current should automatically rise such that high linearity is achieved.

To that goal, Class AB (or B) bias is traditionally employed. It is commonly implemented by an inductor bias feed. Figure 1 illustrates the bias circuit on a common-emitter RF amplifier. The base inductor implements the so-called constant-voltage bias. As input power (P_{in}) increases, the average collector (and base) current will rise while the base-emitter voltage stays constant.

Therefore, what is needed are adaptively biased radio frequency amplifiers using a power detector control circuit and an adaptive bias method for radio frequency amplifiers based on the use of a power detector control circuit to overcome these and other problems associated with the related art.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Figure 1. Depiction of an inductor base bias feed.

Figure 2. Depiction of a self base bias control circuit.

Figure 3. Depiction of a resistor base bias feed.

Figure 4. Depiction of a dual bias-feed circuit.

Figure 5. Depiction of emitter degeneration by inductor and resistor.

Figure 6. Depiction of a WCDMA Two-stage RF driver amplifier.

Figure 7. Depiction of a power detector bias control circuit.

Figure 8. Depiction of an F driver amplifier chip microphotograph.

Figure 9. Graph showing the measured RF driver amplifier current consumption versus input power.

Figure 10. Graph showing the measured gain compression of the driver amplifier versus input power.

Figure 11. Graph showing the measured ACPR of the driver amplifier (P_{out} = 3.5dBm).

Figure 12. Graph showing the measured driver amplifier ACPR results.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to a novel design of a power detector control circuit. It provides current boost to supplement the quiescent current of the RF amplifier at high power level. The circuit is low-power, compact, stable, and digitally programmable. It is capable to provide Class AB-like bias on an amplifier with resistor degeneration. It has been experimentally demonstrated to effectively improve 1dB compression and the ACPR performances on a WCDMA RF driver amplifier without increasing the quiescent current consumption.

The present invention also provides an adaptive bias method for RF amplifiers. Based on a power detector control circuit, the scheme is simple, area-efficient, low-power, stable and digitally-programmable. It is particularly useful when the amplifier features resistive degeneration. The technique is experimentally demonstrated on a RF driver amplifier of a WCDMA mobile phone transmitter. It is shown that the amplifier linearity and compression performances are substantially improved without an increase in the quiescent current. By achieving a RF amplifier with higher average efficiency, the invention would increase the battery life of the wireless device.

The circuit of Figure 2 extends this concept and implements a "self base bias control". The proposed bias circuit, shown in Figure 2, is the combination of a constant base voltage (inductor) circuit and a PMOS current mirror circuit with a constant current source. In the large signal condition, the PMOS current mirror will feed back (and amplify) the increase in base current, thus giving rise to an even higher base current boost. The bias circuit is compact and can be readily integrated. It has demonstrated to increase the amplifier output 1dB compression point (P_{1dB}) by 2.4dB under the same quiescent current. However, the approach is β-sensitive. And because of the inherent current feedback action, it can potentially run into instability. So, stability criteria (which ensure that the final current multiplying ratio is bounded) have to be rigorously ensured under all process and temperature corners.

An integrated base bias inductor consumes a lot of silicon area. Bias feed using a resistor is a common alternative. This is shown in Figure 3. In order to provide adequate RF signal blocking, the resistor (R) is usually designed as several KΩ. Unfortunately, the Class AB action is hindered. It is because any increase in the base current of the common-emitter amplifier would cause a voltage drop at the base. The subsequent base-emitter voltage (V_{be}) compression at large signal condition would greatly limit the current boost. The higher the resistor value, the more the bias circuit resembles a constant-current bias (where the collector current could not rise as P_{in} increases).

To mitigate this, a "dual bias feed" scheme was proposed as shown in Figure 4. As the RF signal increases, the drop on V_{be} will increase the voltage drop across the reference diode and, therefore, increasing its current. This will, in turn, compensate the V_{be} compression and raise the collector current. The scheme was demonstrated on a low-noise amplifier (LNA). It achieved a P_{1dB} improvement of 5dB as compared to a simple resistor feed LNA. The bias is also very compact for integration, and it is more stable than the previous work. However, it lacks the flexibility of programmability, which is necessary to compensate for the inevitable process variations.

For linearity improvement or matching purposes, RF amplifiers commonly employs emitter degeneration as shown in Figure 5. The degeneration can be in the form of an

inductor (L_e) which allows higher (swing below ground) signal handling capability, or a resistor degeneration (R_e) which is far more compact in silicon area. While both schemes mentioned above would provide Class AB action with L_e degeneration, they will fail with R_e. It is because the resistor would raise the emitter voltage (while the base voltage stays constant) as soon as the transistor current starts to rise. The resulting V_{be} compression would then substantially limit the current boost effects.

Thus, the present invention provides an adaptive amplifier bias method based on a "power detector control" circuit. The scheme is simple, area-efficient, low-power, stable and digitally-programmable. Moreover, it functions with amplifiers with either inductor or resistive degeneration. To demonstrate the concept, we have implemented it in the first stage of a WCDMA mobile phone transmitter RF driver amplifier. Those of skill in the art will also find the innovation generally applicable to other types of RF amplifiers design.

Power Detector Control Circuit

Figure 6 shows the low-power driver amplifier for the W-CDMA mobile phone transmitter applications. The amplifier is a two-path two-stage single-ended design. The first stage incorporates a cascode amplifier (for variable gain), while the second stage is a common-emitter (CE) amplifier (for power match). The first and the second stage features resistor and inductor emitter degeneration, respectively. As discussed before, the bias circuits should adaptively adjust current consumption to achieve good linearity performances for large signal condition, and maintain high efficiency during power backoff.

To that end, the CE amplifier, which has an inductor degeneration, employs a conventional constant voltage (Class AB) bias (Bias2). An active buffer circuit is used in place of an inductor to save silicon area. The buffer presents a high impedance at 2 GHz, and a near-zero impedance at dc.

While the active buffer is very effective to provide current boost in the second stage, it will fail in the first stage (cascode amplifier) due to the resistor degeneration. As explained earlier, the emitter resistance will compress the base-emitter voltage as soon as the current goes up, thus substantially limiting the Class AB action.

To achieve an adaptive current bias for the cascode amplifier, we employ a power detector control circuit shown in Figure 7. It senses the differential input signals for the cascode amplifier through two capacitors (C_1, C_2). They are of small values (50fF) to minimize loading to the main cascode amplifier. Simulations show that the gain loss is about 0.2dB, which is deemed negligible.

Signal detection is accomplished by two bipolar devices (Q_1, Q_2) configured as common-emitter amplifiers. They are biased with very low quiescent current (20μA). As a result, their collector currents (I_1, I_2) will be clipped very easily and drastically during large

signal conditions. When that happens, the average current (I_{ave}), or the dc part of the clipped currents, will rise above the quiescent current level (I_{cq}). That is, $I_{ave} = I_{cq} + \Delta I$. The higher the signal level, the bigger the resulting average current.

Notice that the two collector currents (I_{Q1}, I_{Q2}) are differential in nature. While having the same average current, their (RF) signal components are 180° out of phase. Therefore, when the two currents are summed at the drain of transistor M_1, the signal part is eliminated. The current of M_1 (I_{M1}) then contains twice the average current. In summary, I_{M1} is proportional to the input signal level.

When such heavy current clipping occurs, a host of harmonic and intermodulation distortion components are generated. Signal combinations at the drain of M_1 would remove, to the first order, all the even-order distortions. However, the odd-order components would stay (with the dc component, I_{ave}). If I_{M1} is directly fed back to the main cascode amplifier to supplement its quiescent current (I_{cq1}), the distortion components will modulate with the RF signal and degrade the amplifier linearity performances. So, they need to be adequately filtered.

Lowpass filtering is carried out on the current I_{M1} by a single pole located between the gates of M_1 and M_2. The values of R_{lp} and C_{lp} are selected such that the pole frequency is low enough to provide sufficient rejection to the distortion components. However, if the pole frequency is set too low, the average current will not response fast enough with the signal envelope, defeating the purpose of the adaptive bias control. In our WCDMA amplifier where the signal bandwidth is about 5MHz, the pole is set at 1.4MHz (with R_{lp} = 18KΩ, C_{lp} = 6.4pF). Simulations and experimental results have confirmed it is a good compromise between good distortion removal and fast envelope tracking.

After the low-pass filtering, I_{M1} is mirrored to the drain of M_2 with a 1:1 ratio. The quiescent current ($2I_{cq}$) is to be subtracted at the collector of Q_3. The resulting current is delivered to the collector of transistor Q_4. The Q_4 collector current, I_{Q4}, equals $2I_{ave} - 2I_{cq} = 2\Delta I$. At this point, we have derived a dc current (I_{Q4}) which is directly proportional to the amplifier input level P_{in}. The core signal detection operation is accomplished.

The current I_{Q4} is then mirrored by Q_4 and Q_5. The current mirror ratio of 1:4 will magnify the current boost effects of the power detector control bias on the cascode amplifier for a given input level. Transistor pair M_3-M_4 will then reverse the direction of the current flow, and deliver the dc current to supplement the quiescent current (Icq1) at the bias network the cascode amplifier.

The mirror ratio between M_3 and M_4 is designed to be digitally programmable. This allows flexibility and controllability to the current boosting effects on the amplifier to account for process and temperature variations. The total transistor size of M_4 is eight times bigger than that of M_3. Depending on a 2-bit digital control, either 8, 6, 4, and 0 units of M_4 can be

disconnected. Therefore, the mirror ratio can be digitally programmed to be either 1:0 (which effectively disables the power detector control circuit), or progressively increase to 1:2, 1:4 or 1:8. In summary, the power detector control can supplement the quiescent current of the cascode amplifier by 0, 16, 32 or 64 times ΔI, where ΔI is proportional to P_{in}.

Since current boost is not dependent on the amplifier base current or the output power, there is no feedback, and the scheme is inherently stable. The circuit consumes low-power (dc current of 200μA), and is compact in silicon area. As will be illustrated in the next section, the power detector bias control is effective to enhance the amplifier linearity at high output power level, without increasing the quiescent current consumption at small signal level.

Experimental Results

The driver amplifier is fabricated in IBM's 0.25um SiGe BiCMOS process. It measures 2x0.9mm^2. The chip microphotograph is shown in Figure 8. The power detector bias circuit is very compact. It measures 0.5x0.1mm^2, or only 3% of the total amplifier area.

The measured amplifier gain is 16dB. It consumes a total quiescent current of 9mA (differential path) under 2.7V supply. Figure 9 displays the measured current consumption of the amplifier versus input power. Additional current is provided to the cascode amplifier when the detector current mirror ratio is enabled, verifying the adaptive bias's correct functionality and programmability. Figure 10 shows the resulting amplifier gain compression. Due to the dynamic bias, the gain compression is compensated by the gain expansion. It significantly improves the output 1dB compression point by 3.5dB (from 9.2 to 12.7dBm).

The dynamic bias scheme also improves the RFVGA linearity. Figure 11 shows the output spectrum with an actual W-CDMA signal at the maximum average power level of 3.5dBm. The 3rd- and the 5th-order intermodulaton distortion products would cause adjacent channels to appear at 5 and 10MHz offsets. These "skirts" get reduced when the detector is turned on. The higher the current boost, the lower they become. The detector circuit has improved the adjacent channel power ratio (ACPR) by 6dB, and the measured ACPRs at 5 and 10MHz equal -43 and -59dB, respectively. They meet the specifications (-33 and -43dB) with comfortable margin. The measured ACPR at 5MHz offset versus output power is plotted in Figure 12. The power detector bias control scheme is providing linearity improvements over a wide range (10dB) of output levels.

In conclusion, the power detector control circuit described in this Disclosure is shown to be a very effective way to improve amplifier linearity without increasing the amplifier quiescent current. By sensing the input power and providing current boost to the amplifier at high signal level, it improves the linearity and compression performances without increasing the quiescent bias current. The adaptive bias circuit is low-power, compact, and is perfectly

suitable for silicon integration. Since it only senses the input power and not the base current, it is stable and beta-insensitive. The scheme is digitally programmable, and provides Class AB-like bias even to an amplifier with resistive emitter degeneration. Those of skill in the art will recognize that the present invention will find applications in RF amplifier design where high linearity is to be achieved with good efficiency. It is particularly useful when digital programmability is desired, or the amplifier features resistive emitter degeneration.

Other Embodiments

The detailed description set-forth above is provided to aid those skilled in the art in practicing the present invention. However, the invention described and claimed herein is not to be limited in scope by the specific embodiments herein disclosed because these embodiments are intended as illustration of several aspects of the invention. Any equivalent embodiments are intended to be within the scope of this invention. Indeed, various modifications of the invention in addition to those shown and described herein will become apparent to those skilled in the art from the foregoing description which do not depart from the spirit or scope of the present inventive discovery. Such modifications are also intended to fall within the scope of the appended claims.

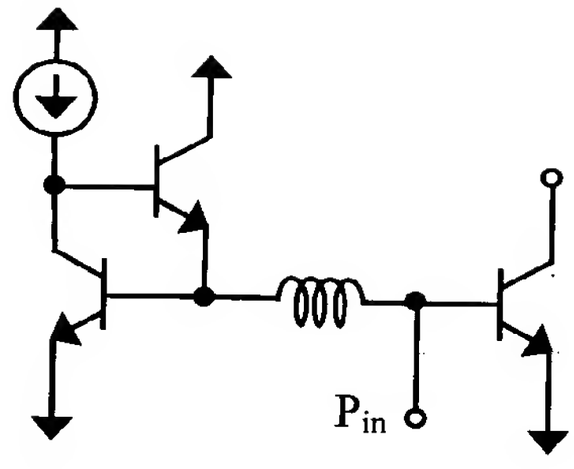
References Cited

All publications, patents, patent applications and other references cited in this application are incorporated herein by reference in their entirety for all purposes to the same extent as if each individual publication, patent, patent application or other reference was specifically and individually indicated to be incorporated by reference in its entirety for all purposes. Citation of a reference herein shall not be construed as an admission that such is prior art to the present invention. Such references include:

1. S. Shinjo, K. Mori, H. Joba, N. Suematsu, T. Takagi, "Low quiescent current SiGe HBT driver amplifier having self base bias control circuit," IEICE Trans. Electron., vol. E85-C, no. 7, pp. 1404-1411, July 2002.

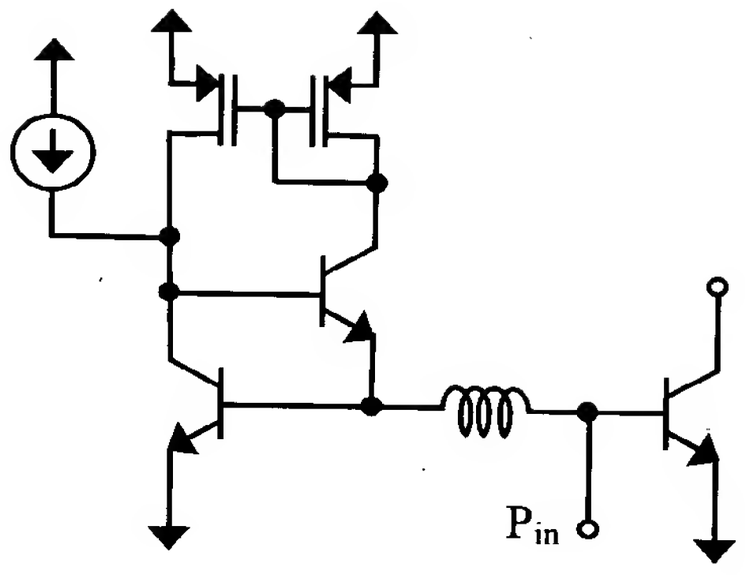
2. E. Taniguchi, T. Ikushima, K. Itoh, N. Suematsu, "A dual bias-feed circuit design for SiGe HBT low-noise linear amplifier," IEEE Trans. Microwave Theory Tech., vol. 51, no.2, pp. 414-421, Feb. 2003.

FIGURE 1



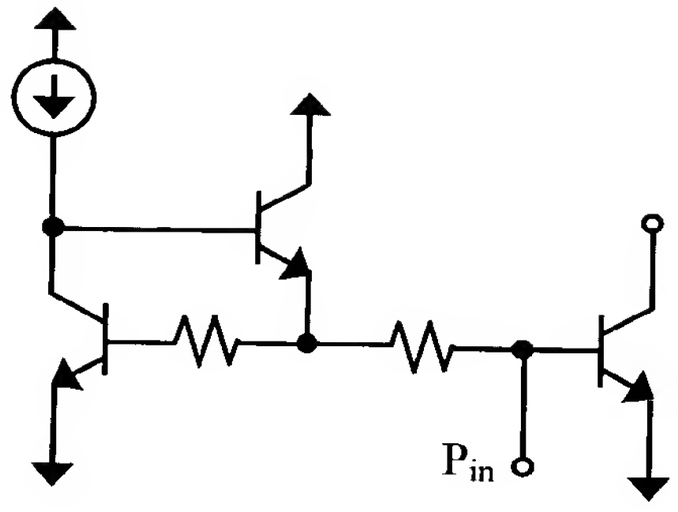
Inductor base bias feed

FIGURE 2



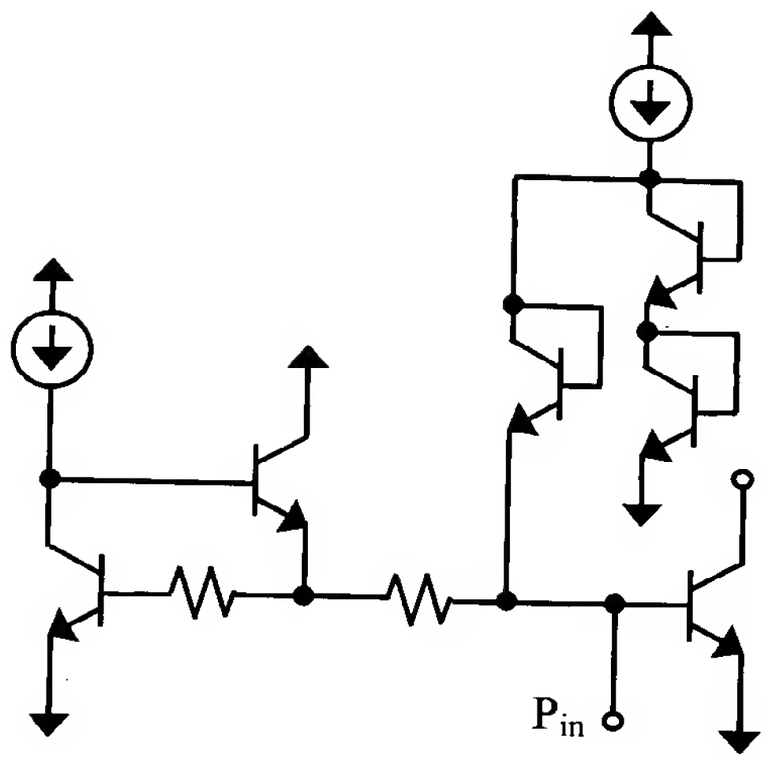
Self base bias control circuit

FIGURE 3



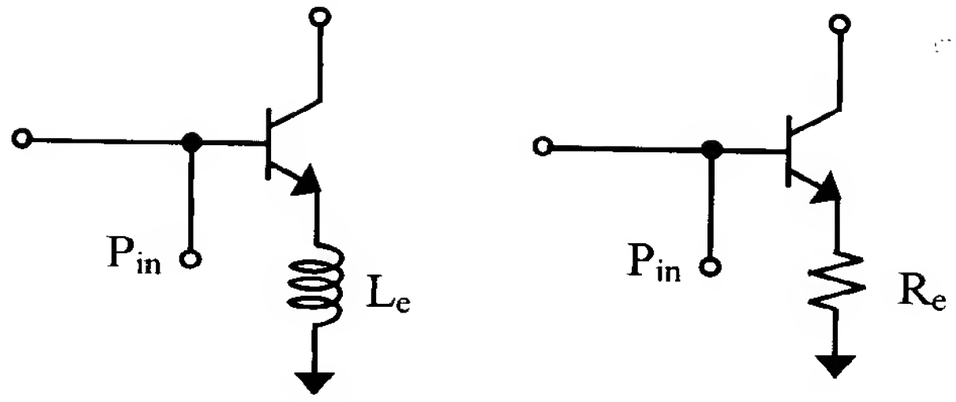
Resistor base bias feed

FIGURE 4



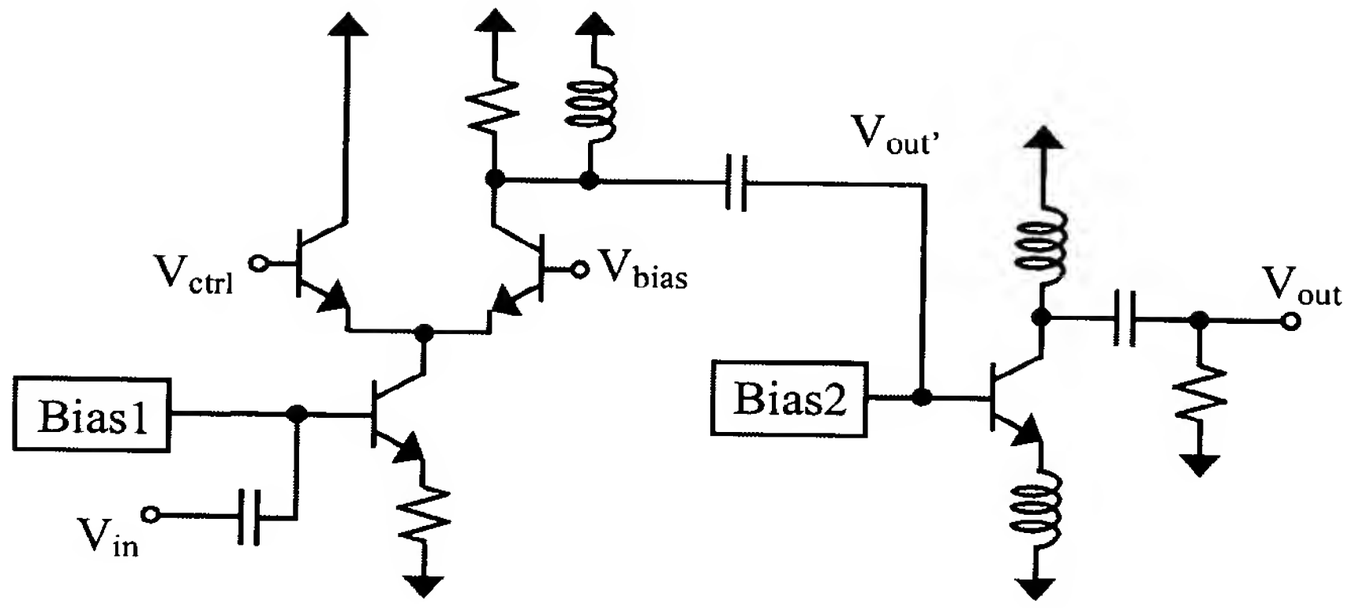
Dual bias-feed circuit

FIGURE 5



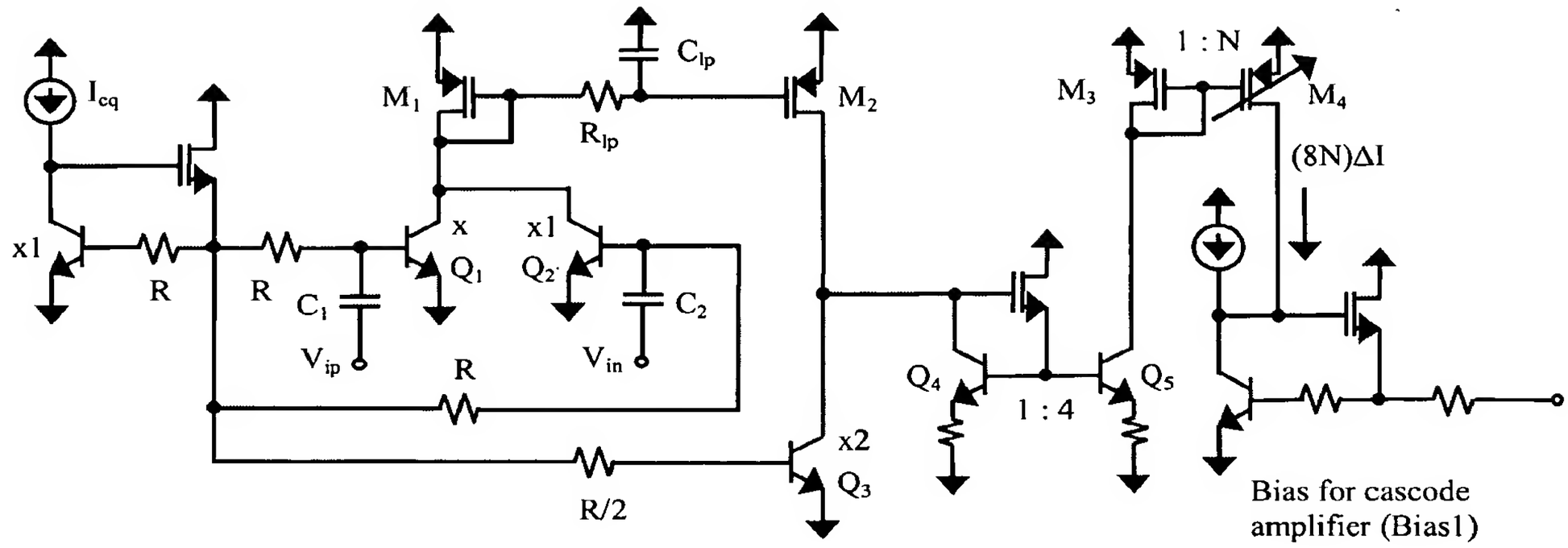
Emitter degeneration by inductor and resistor

FIGURE 6



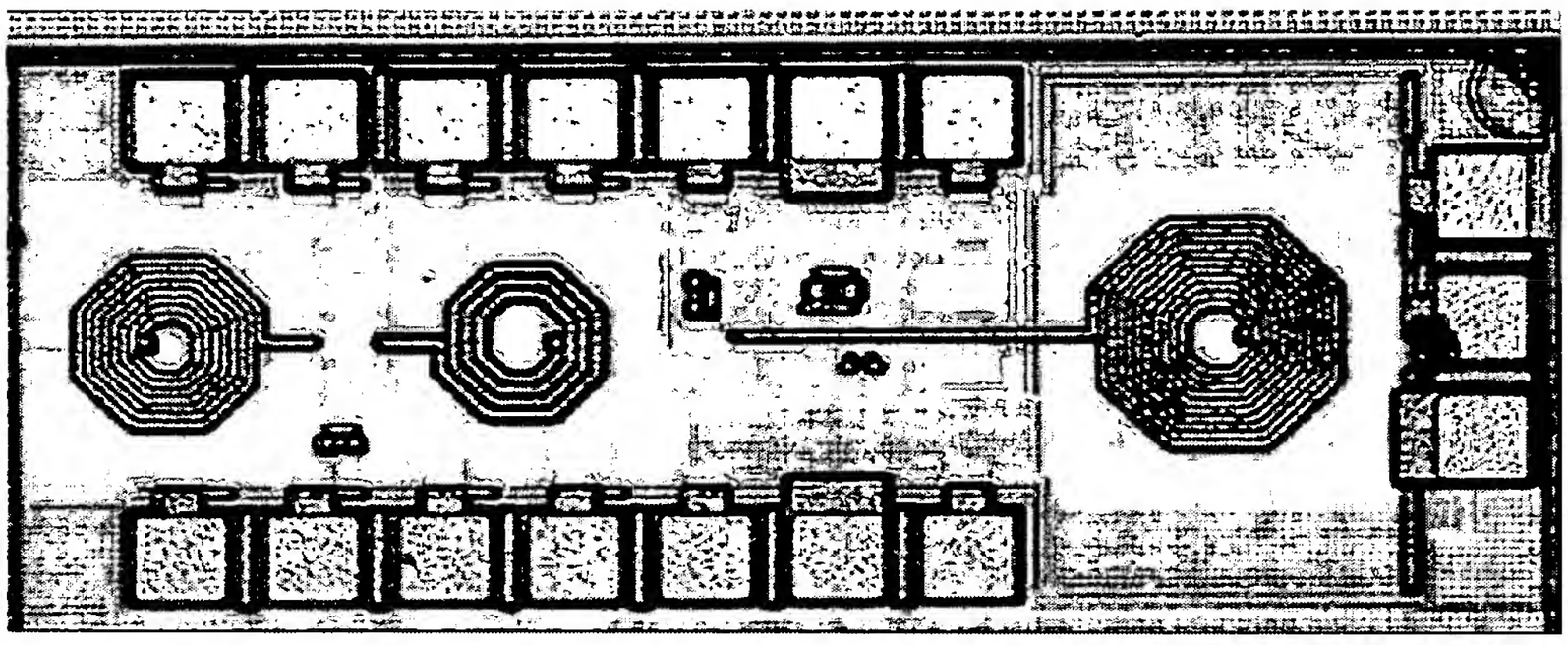
WCDMA Two-stage RF driver amplifier

FIGURE 7



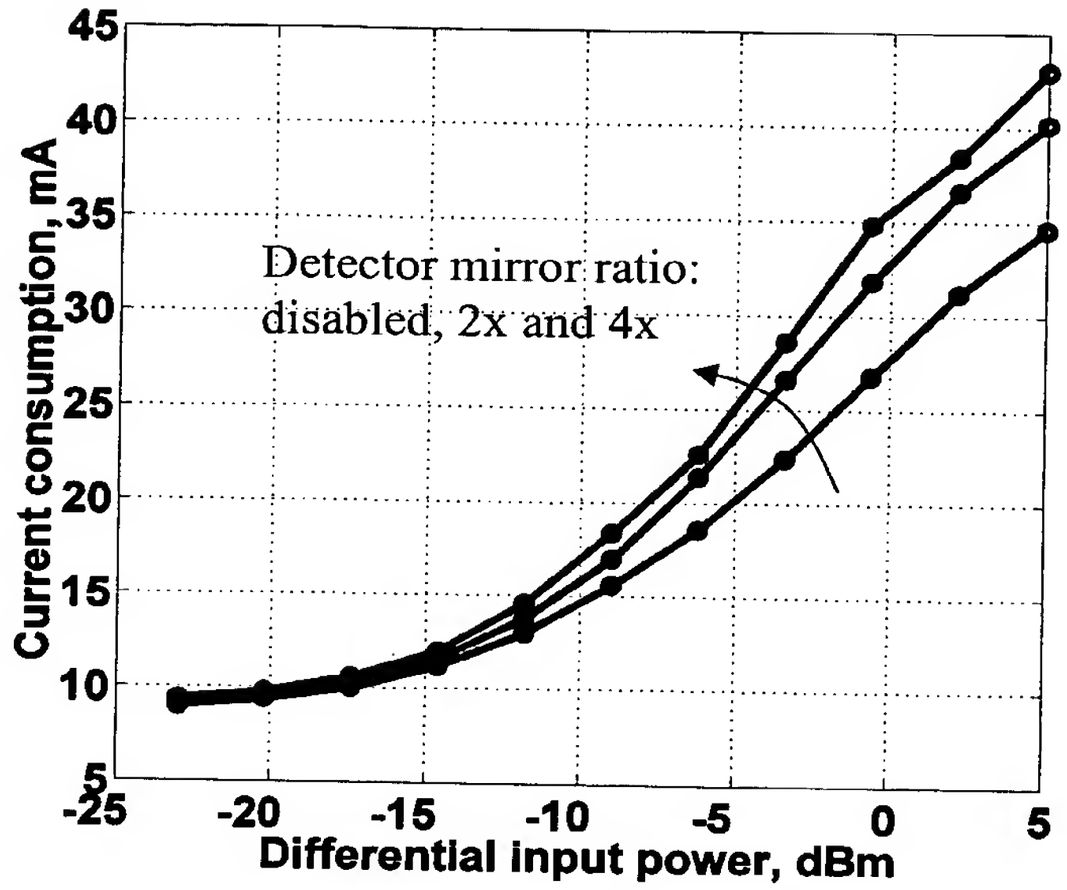
Power detector bias control circuit

FIGURE 8



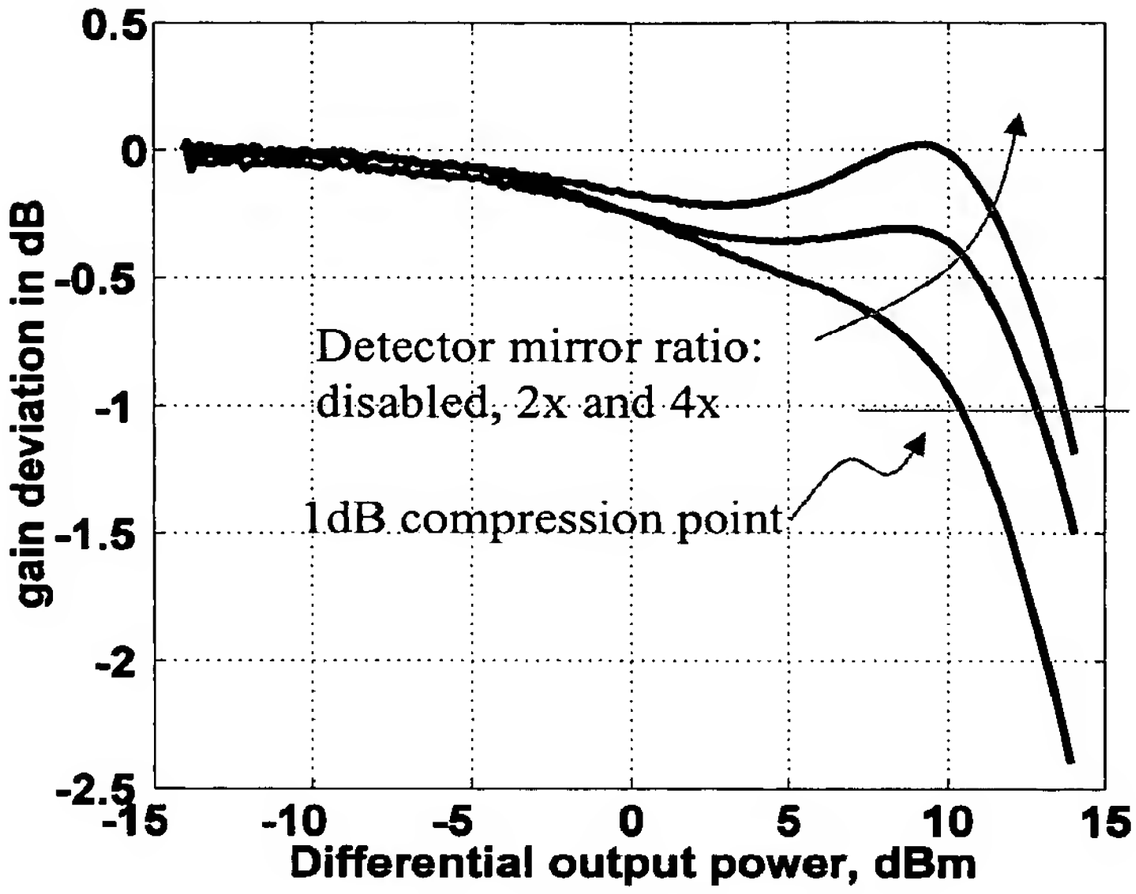
RF driver amplifier chip microphotograph

FIGURE 9



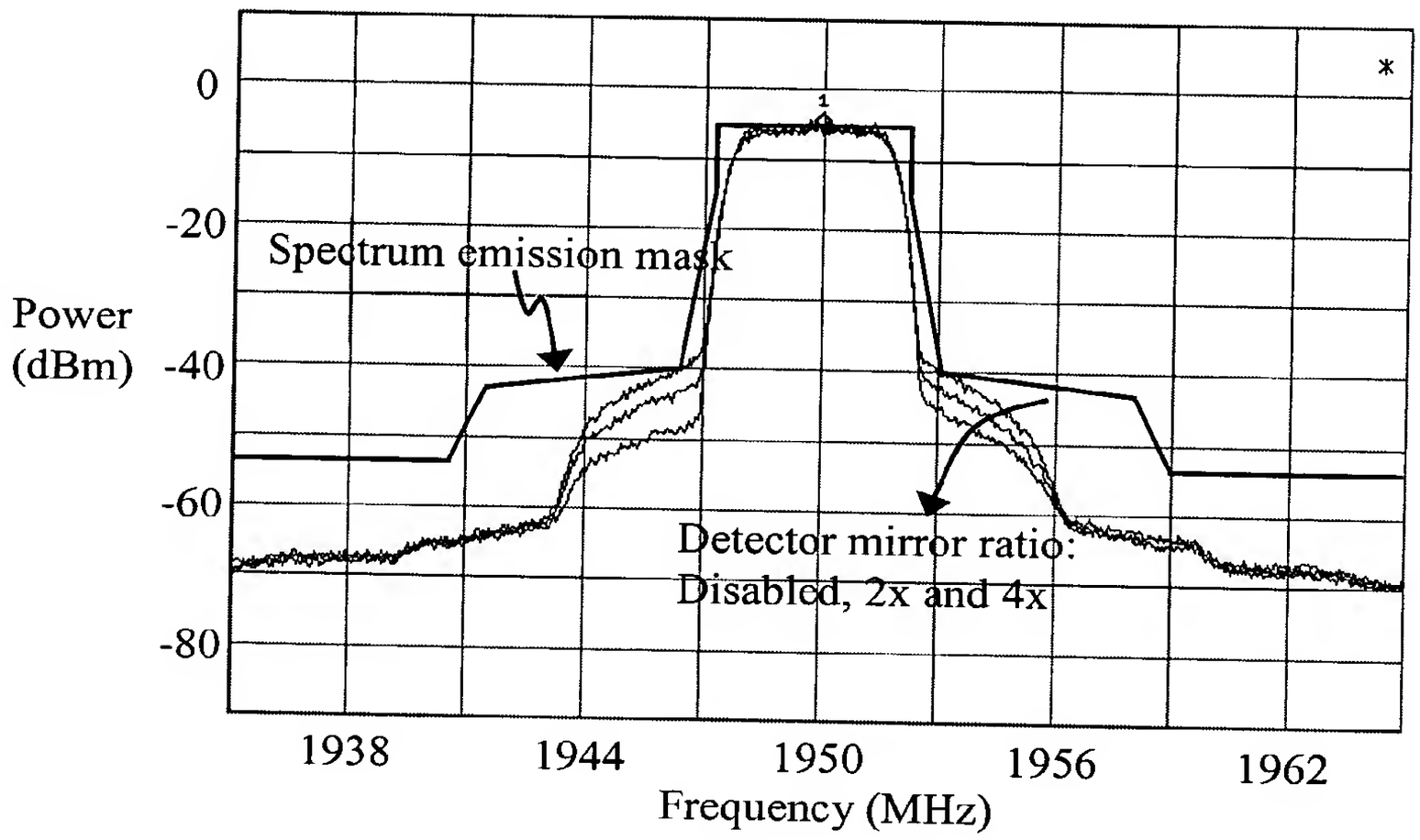
Measured RF driver amplifier current consumption versus input power

FIGURE 10



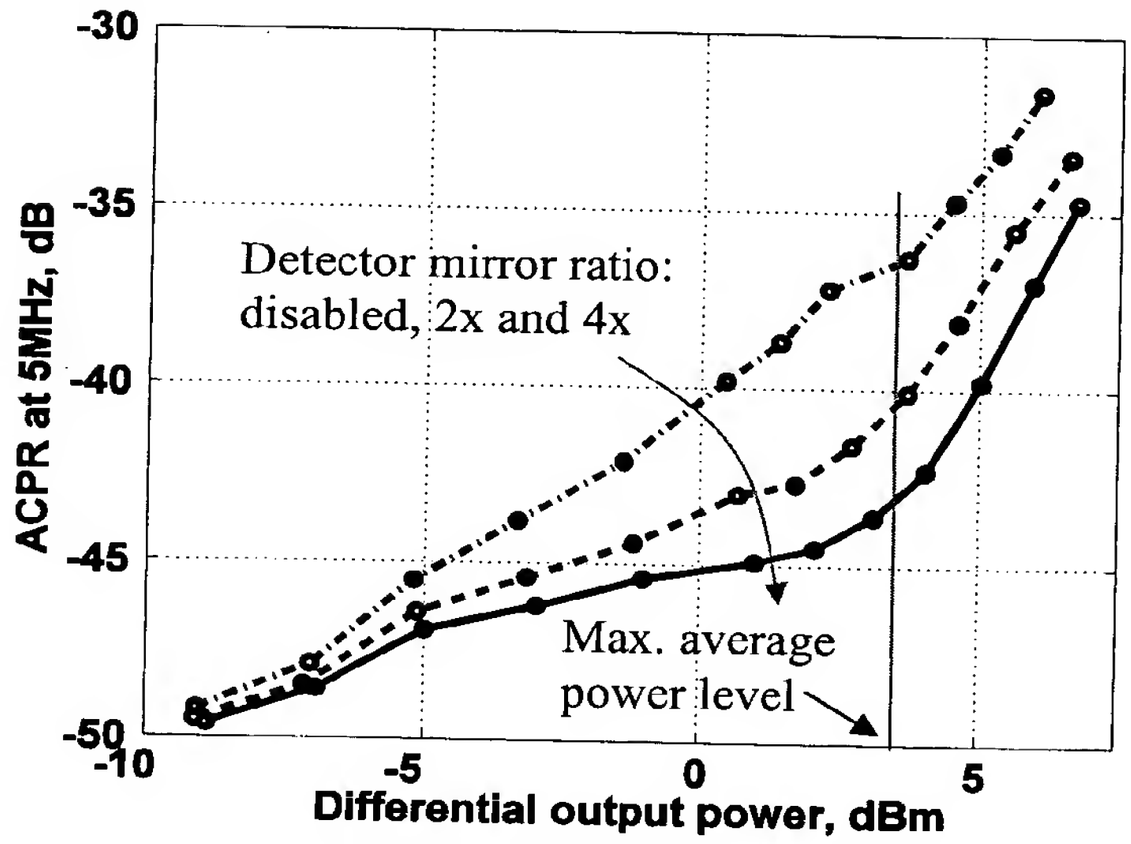
Measured gain compression of the driver amplifier versus input power

FIGURE 11



Measured ACPR of the driver amplifier (P_{out} = 3.5dBm)

FIGURE 12



Measured driver amplifier ACPR results

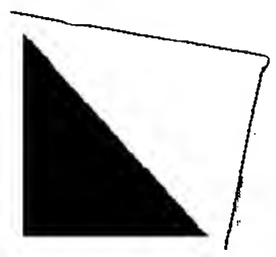
APPLICATION DATA SHEET

Application Information

Application Type::	Provisional
Subject Matter::	Utility
Number of Copies of CDs::	
Sequence Submission?::	Yes
Computer Readable Form?::	Yes
Title::	**ADAPTIVELY BIASED RF AMPLIFIER USING A POWER DETECTOR CONTROL CIRCUIT**
Attorney Docket Number::	60021010-0036
Request for Early Publication?::	No
Request for Non-Publication?::	No
Total Drawing Sheets::	12
Small Entity?::	Yes
Petition Included?::	No
Secrecy Order in Parent?::	No

Applicant Information

Applicant Authority Type::	Inventor
Primary Citizenship Country::	US
Status::	Full Capacity
Given Name::	Vincent
Middle Name::	W.
Family Name::	Leung
City of Residence::	San Diego
State or Province of Residence::	CA
Country of Residence::	US
Street of Mailing Address::	8840 Costa Verde Blvd., #3312
City of Mailing Address::	San Diego
Postal Code of Mailing Address::	92122



Applicant Information

Applicant Authority Type::	Inventor
Primary Citizenship Country::	US
Status::	Full Capacity
Given Name::	Prasad
Middle Name::	S.
Family Name::	Gudem
City of Residence::	San Diego
State or Province of Residence::	CA
Country of Residence::	US
Street of Mailing Address::	8014 Avenida Navidad, #50
City of Mailing Address::	San Diego
Postal Code of Mailing Address::	92122

Applicant Information

Applicant Authority Type::	Inventor
Primary Citizenship Country::	US
Status::	Full Capacity
Given Name::	Lawrence
Middle Name::	E.
Family Name::	Larson
City of Residence::	San Diego
State or Province of Residence::	CA
Country of Residence::	US
Street of Mailing Address::	9500 Gilman Drive EBUI/Rm 3808 Mail Code 0407
City of Mailing Address::	San Diego
Postal Code of Mailing Address::	92093

Correspondence Information

Correspondence Customer Number::	26263

Domestic Priority Information N/A

Assignee Information

Assignee Name::	The Regents of the University of California